Configurable FPGA-Based Firing Circuit for Single/Three Phase AC Controller

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Abstract

In this paper, a configurable single chip firing circuit for three phase motor speed control based on Field Programmable Gate Array (FPGA) hardware architecture is presented. The proposed circuit is designed, implemented and tested using MAX II PLD chip (EPM1270F256C5 device). The system has the advantages of being simple, flexible and low development cost with built-in self test. The experimental results carried out using Altera development kit showed that the proposed scheme works properly.

I. Introduction

In the last decades, the production of static power electronics switches has been plentiful and diverse. Some of these switches are GTO's biboplar power transistors, MOSFET's, IGBT's and MCT's [1,2]. Even with these devices, the basic thyristor still constitutes a robust, simple and economical devices, that has many applications. Thyristors are widely used in ac voltage controllers for control of power in both AC and DC systems. This is due to their several advantages such as relatively small size, low losses and fast switching. Apart from many uses, ac controllers are industrial heating, light control, transformer tap changing, ac to dc conversion, reactive power compensation and starting as well as speed control of AC motors [1-4]. The main control technique used in ac controller is the phase angle control technique (PAC). The circuit of PAC consists mainly of two antiparallel thyristor switches, connected in series with each line of the ac supply. PAC is low in cost, simple and by which a large amounts of electric power can be economically controlled. The most main part of the PAC circuit is its firing circuit.

In this paper a new scheme is developed and described, for the thyristor firing circuit. The scheme has the advantages of being simple, flexible and low development cost with built-in self test. Also the scheme can be used for single phase and three phase PAC applications.

II. Scheme Development

As shown in the functional block diagram of Fig.1 the single chip firing circuit scheme is operated by 66 MHz master clock and has a system reset input for system initialization.

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The zerocrossing (squared-up supply frequency) input received from one of the power line phases is used to generate the other two phases. The circuit outputs six different pulses for the positive and negative half-cycles of the three phases. The circuit provides self-test feature as system diagnosis routine. It generates the three zerocrossing digital pulses corresponding to the three phases internally. Moreover, a one Hz pulse ouput is produces and connected to a light emmiting diode (LED) so that its visual blinking is indicating that the circuit is responding and functioning properly, specially during the configutration and programming down loading. The firing angle phase shift is preselected to a default maximum value of 180°, during the initialization phase. This phase shift can be decreased in steps via an external switch to the minimum value of 0° degree. The full block diagram of the proposed firing scheme composed of six different units:

- Timing clocks generator.
- One and 60 Hz circuit.
- Firing angle phase shift circuit.
- Positive / Negative delay circuit.
- The phase generator.
- The main firing circuit unit.

The timing clocks generation unit is responssible for initializing the system, generating several clock pulses used for synchronization purposes, produces the enable signals and loads the proper time constants that are required by the other modules. The one and 60 Hz circuit has two functions for board self-testing purposes. It generates the one second blinking pulse which is connected to the LED indicating that the board is responding to the configuration programming during software down loading. The other one is the artificial 60 Hz zerocrossing that enables the user to test board the circuit board without connecting the firing circuit to the power supply. It is composed of several divide by *N* cascaded counters and controlled by the timing circuit.

The firing angle phase shift generator unit is to produce the required time delay(α) between the zerocrossing of the particular line phase and the generated firing pulse in degrees. The phase shift ranges from 0° degree to 180° and in approximatly 0.71° resolution steps. The delay steps are controlled by an external push-botton switch (CNT_EN) which in turn, decrements another counter where its contents is used as a time constant for the phase shift counter.

The POS/NEG delay circuit is introduced to generate a certain short time dealy between the rising and falling edges of the positive and negative firing pulses for the

corresponding phase respectively. This time dely is shown in the timing diagram of Fig.2. This introduced short time delay will prevent the short or open circuits on the power side caused by the high state overlapping due to the opto-couplers time delay response. The delay time depends on the specifications of the opto-couple used. It is in the range of tens of microseconds, therefore, this time delay is kept flexible and can be easily modified by the user to make the firing circuit compatible to any type of opto-coupler switch used.

The phase generation circuit task is to produce internally the other two zerocrossing signals representing the phases Y and Z from the external phase X or from the internal artificial phase in the case of the self test mode . It is mainly composed of several cascaded counters that generate 120° phase shift for both positive and negative half cycles for Y and Z phases. The firing circuit generation unit is considered as the heart of the proposed system. Its main task is to generate the six firing pulses for the positive and negative of the three phases. It is triggered by the external phase applied to the firing chip and controlled by the timing circuit. In the self-test mode, the circuit will be triggered by the self generated zerocrossing pulse.

III. Design of the firing circuit

The proposed firing circuit has been designed, synthesized, and simulated using Altera Quartus software package. It provides a complete design environment for system-on-programmable-chip (SOPC) design. The package offers a very rich library of parameterized modules (LPM) that can be utilized to construct most of the various counters and sequential circuits used in this design. The schematic (Block) editor is used to desribe the design subsystems as modules. The complete design has been designed and synthesized around FPGA chip. FPGAs are platforms that can be used to design a specific hardware optimized to implement specific digital circuits. Thay are considered to be uncommitted ‘sea of logic gates” that can be programmed by connecting the logic gates together to form ant desired digital component such as registers, counters, arithmetic logic units, and so foth. They have a significant advantage of being reconfigurable directly by the software. This adds flexibility in designing the hardware and updating its structure. The programmability, flexibility, prformance, and potential for lower cost have opened up new avenues for FPGAs to be used in a broad range of applicatopns[5].

The time simulation option offered by the software package is a powerful tool for testing and evaluating the logical and arithmetic operations and the limitations for internal timing of the design. It enables the designer to verify the system performance before it is actually committed to real hardware. In fact, it reduces the time required to transform the initial design concept into working silicon drastically.

The proposed firing circuit is designed as individual sub-modules in a hierarchal manner which enables the designer to test the various units individually. The Quartus software package provided by Altera is used to design and simulate the proposed firing circuit. The design has been implemented around MAX II PLD chip (EPM1270F256C5 device) [6].

IV. Experimental test

A low cost simple development board included with the MAX II development kit (EZ1CUSB) based on the EPM1270F256C5 device is used. It is a ROM-based (non-volatile) full- featured platform for prototyping and evaluating designs based on programmable logic devices. It operates by 66 MHz clock and the configuration programs can be down loaded from the PC via JTAG interface and parallel port [7].

The prototype set up for the proposed scheme of the firing circuit has been implemented, verified and tested. Fig.3 (a) and (b) shows the display output for the logic analyzer for the firing pulses generated for positive and negative cycles of the three phases when α equal to 115° and 22° respectively.

V. Conclusion

In this paper, a novel configurable hardware implementation single chip firing circuit firing circuit for three phase motor speed control based on (FPGA) hardware architecture is presented. The system has the advantages of being simple, and flexible with built-in self test and low development cost. The performance of the prototype hardware set up proved the concept of the proposed circuit. The system is implemented using MAX II FPGA chip. This programmable hardware environment will give the design the possibility to be applied for further applications.

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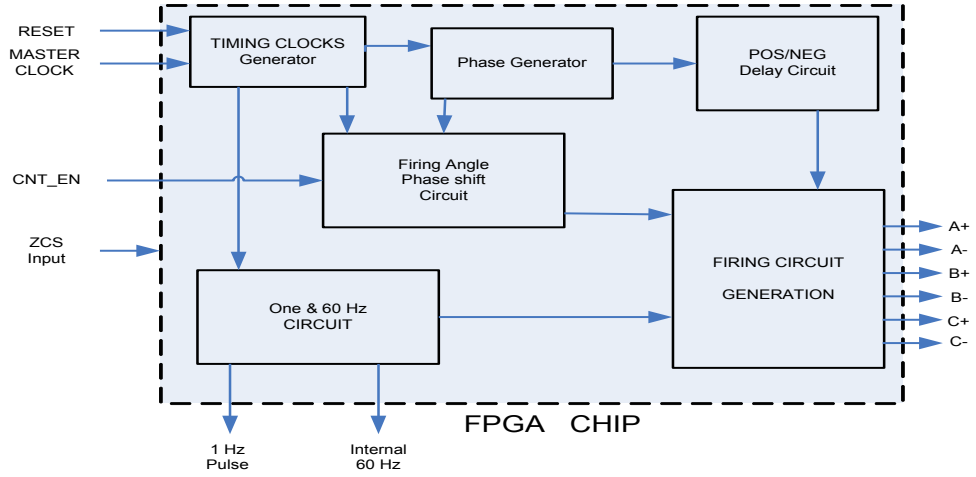


Fig.1 Functional bock diagram for the proposed firing circuit.

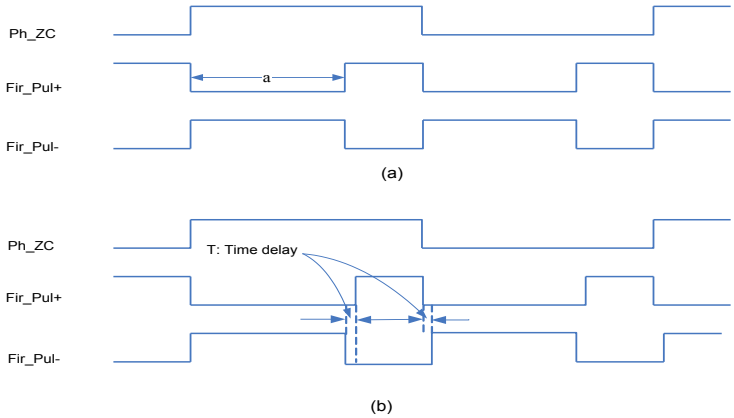
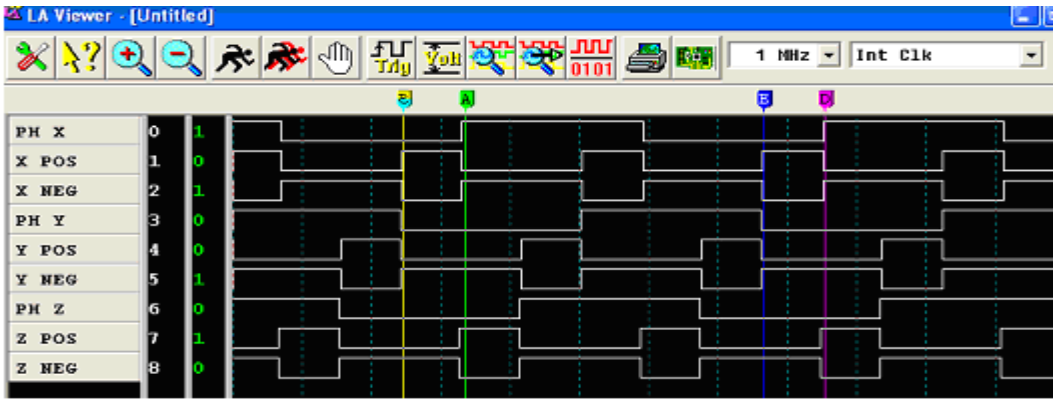
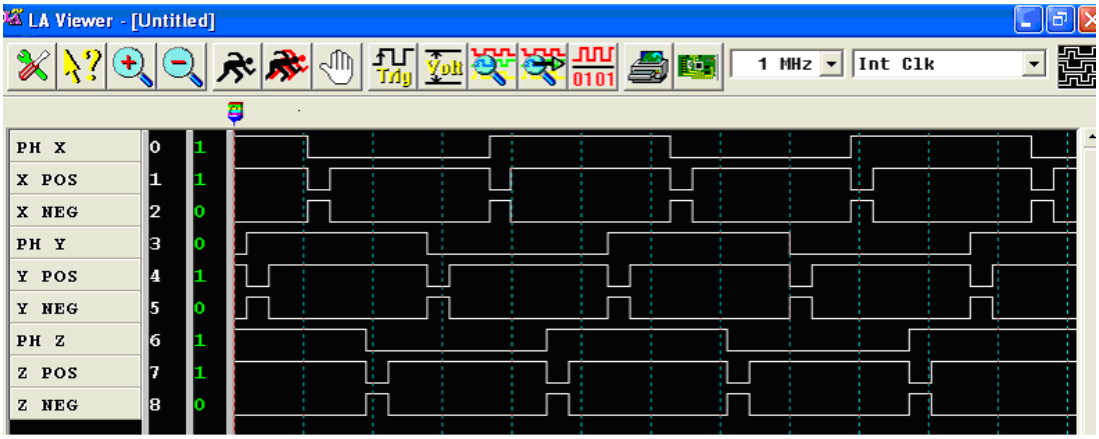


Fig. 2: Timing diagram showing the pos/neg pulses edge delay (a) Without delay b) With some delay



(a)



(b)

Fig.3 Logic analyzer output p of the firing pulses (a) $\alpha = 115°$ (b) $\alpha = 22°$