Predicting system level ESD performance

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ABSTRACT

This paper presents an ESD circuit model for a complete system, which allows accurate prediction of system pass levels during a system level ('ESD gun") test. The paper presents a Spice model for the ESD gun and a Verilog-A model for the protection device, both on-chip and on-board. Magnetic field scanning during an ESD discharge is used to optimize the model.

INTRODUCTION

Since electronic systems are used in electrostatically unprotected environments, such as an end user's home, it is important for system vendors to be able to predict the system-level ESD pass level, which is usually measured according to IEC 61000-4-2 (IEC 2008). Unfortunately, typical ESD conditions fall outside the range of small-signal parameters for which well-calibrated component models are readily available. This has given the field of ESD over the years a touch of 'black magic' among electronic engineers. In order to remedy this situation, the JEDEC organization has published two white papers (JEP161 2011, JEP162 2013) on system level testing, which describe a modeling approach which is called 'System-efficient ESD Design' (SEED).

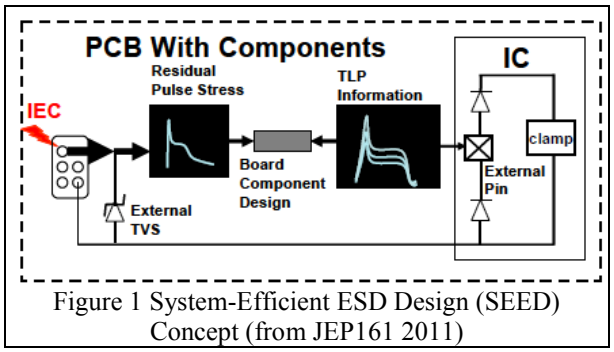

Figure 1 System-Efficient ESD Design (SEED) Concept (from JEP161 2011)

Figure 1 illustrates the basic concept. When a system-level pulse ('IEC' pulse) enters a system, by firing an ESD gun into a specified port, the main ESD current is supposed to flow into the external TVS, but inevitably a small residual current will flow into the IC, which may cause an over-voltage there. Either the residual current may cause thermal damage to the IC or the resulting over-voltage may damage sensitive gate oxides in the IC.
It is the goal of SEED to simulate the residual current and over-voltage with sufficient accuracy to allow an accurate prediction of the system failure level.
For a valid prediction, it is important to assess the impact of the parasitics in the system (Johnsson et al. 2012, Notermans et al. 2016), in particular of inductances. Furthermore, it is essential to have proper clamp models. This paper will focus on the development of proper clamp models, using Verilog-A, which allow a flexible implementation in a circuit simulation environment, such as ADS. Suitable models will be described in the modeling section. In the calibration section, the impact of parasitics will be explored and proper ways to extract the parameter values will be proposed. The application of the methodology on a USB3 interface board will be described. Finally, the use of an H-field scanning tool to optimize the system model is discussed.

MODELING INDIVIDUAL COMPONENTS

A full system model according to SEED needs at least three components: A gun model, a model for the external clamp, and a model for the parasitics on the system board and the IC receiving pin.
Note that the model of the IC pin does not need to include any (possibly proprietary) information on the layout or function of the IC I/O circuitry. The residual current is completely defined by the internal IC protection. For a SEED model, it is sufficient to characterize the I-V curve in the ESD timeframe, which will be described in the calibration section.

Gun model

The gun generator model (Figure 2) is derived from the work of (Wang et al. 2003) and (Caniggia et al. 2006).

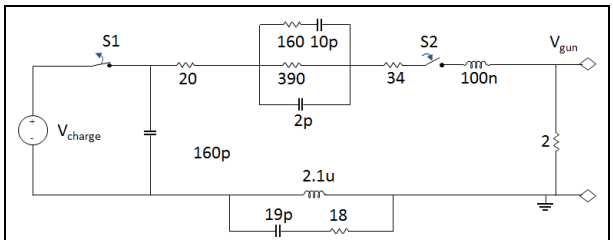

Figure 2 ESD Gun Model

Several workers have implemented similar gun models with small variations (Yang 2018). For our purpose, we optimized the model to generate a worst-case pulse with the minimum rise-time of about 0.6 ns and a high first peak of about 4 A. Furthermore, we tried to strike a balance between the waveforms measured with different guns. Figure 3 shows a simulated current waveform

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compared to a measured waveforms from a NoiseKen ESS-S3011A and a Schloeder SESD 30000 gun. The relatively wide IEC 61000-4-2 specification is indicated as a hashed band. The simulated and Noiseken waveforms are in spec. The Schloeder guns is slightly out of spec in the second, slower peak. The simulated waveform is about midway between the two extremes in the second peak.

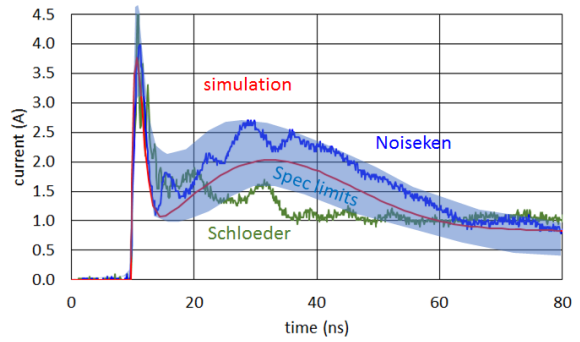

Figure 3 Simulated and Measured Waveforms

Clamp models

Verilog-A uses a reduced syntax from Verilog-AMS. It is integrated in Keysight's Advanced Design System (ADS®). Verilog-A offers a flexible and simple way to implement diodes and snapback devices, with and without hysteresis. The clamps are modeled using a quasi-static, piecewise linear (PWL) I-V curve. Because the derivative at the inflection points of such a curve is not continuous, convergence problems cannot be avoided completely.
An advantage of piecewise linear curves is the ease of calibration. All that is needed to calibrate the model is to enter the measured (V,I) values for each of the inflection points.

Diode model
The simplest possible form describes a non-ideal (avalanche) diode, defined by the inflection points Von, Ion, Ron for forward polarity and Vrev, Irev, Rrev for reverse polarity (Figure 4). This model is suited for clamps that do not exhibit snapback.

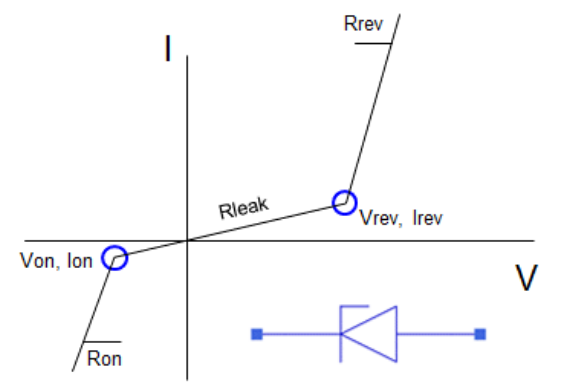

Figure 4 Piecewise Linear Model without Snapback

Snapback model
The clamp model can be extended in a straightforward manner to include snapback (Figure 5). Two additional inflection points are defined: [Vt1, It1] and [Vh, Ih]. The clamp triggers at [Vt1 It1] and for I>It1 it will enter its low-impedance state (given by Rrev). The minimum voltage and current for this low-impedance state are defined by [Vh,Ih]. Once I<Ih the clamp will return to its high-impedance state.

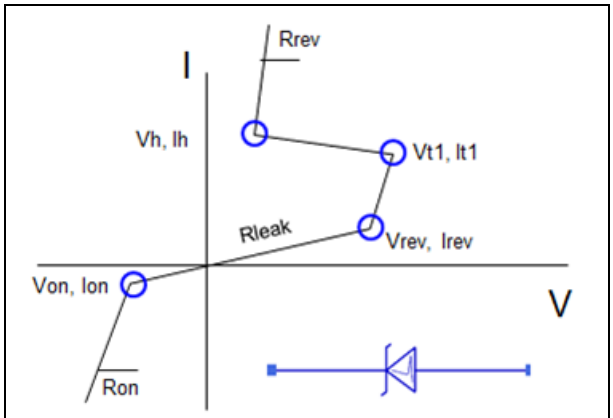

Figure 5 Piecewise Linear Model with Snapback

Note that the same curve is traversed when the current is increasing or decreasing (no hysteresis). In other words, the function is single-valued in current. In reality, Ih<It1 always, but the error introduced by the simplification Ih>It1 is small, because both Ih, It1 << It2.
Note further that Vrev and Vt1 are distinct. Vrev is the voltage at which the clamp leaves its high-impedance state and starts to conduct, typically when a trigger device kicks in. Snapback to the low-impedance state occurs at [Vt1, It1], when the main clamp triggers.
Forward (on) and reverse (rev) polarity are defined in accordance with the definitions for a zener diode.

Hysteresis
Depending on the timescale, the protection device may exhibit hysteresis. For instance, an SCR may need some conductivity modulation to enter its low-impedance state.

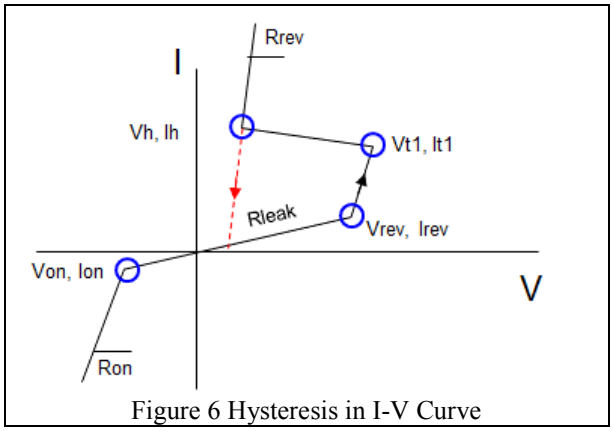

Figure 6 Hysteresis in I-V Curve

When switching off such a device, the charge takes some time to disappear and the SCR remains triggered for a

long time, typically microseconds. In the I-V curve, this effect manifests itself as a hysteresis (Figure 6).
When the current is increasing, the I-V curve follows the branch via Vrev, Irev and Vt1, and It1, which corresponds to the triggering of the protection. When the current is decreasing, the high-current curve with resistance Rrev is followed, i.e. the current just fades away'. without voltage increase (to Vt1). It is important to add this distinction to the model, since otherwise an unrealistic voltage overshoot would also appear at the end of pulse (Figure 7 red solid line), when the device is triggered by a square current pulse. With current hysteresis, the voltage waveform only shows an overshoot at the beginning of the pulse (Figure 7 blue dashed line), which is accurate at short (ESD) timescales.

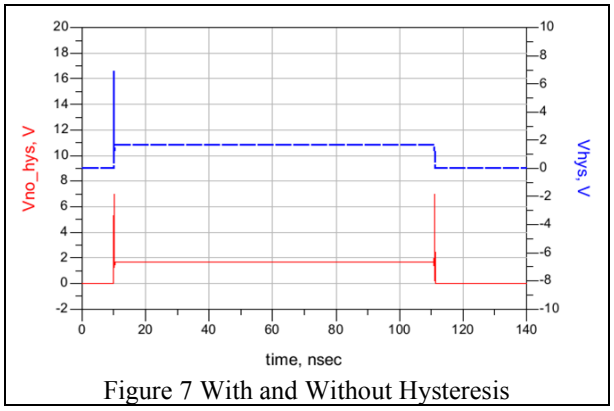

Figure 7 With and Without Hysteresis

Note that the hysteresis only occurs for timescales shorter than the time it takes to remove the injected charge of the device, which is around 10 µs. For longer timescales, notably during DC simulation, the hysteresis does not occur. This timescale dependence also needs to be taken into account in the model.

Dynamic overshoot
Dynamic effects due to metal inductances are implemented by adding a small inductance of about 2 nH in series to the Verilog-A model, which accounts for the L.dI/dt overshoot. The additional overshoot due to conductivity modulation can also be modeled by current-dependent resistor (Manouvrier et al. 2008), but this extension is out of scope for this paper and will be reported elsewhere (Notermans et al. 2018).

System model

Typical systems comprise a processor IC with its internal protection, an external protection, and a system PCB which may contain several parasitic components (Figure 8). The internal protection of the IC is modeled in the same way as an external clamp. The parasitic board components are represented as lumped elements. For high-speed applications, capacitors are typically very small (< 1 pF) and they may be left out of the SEED simulation.
Figure 9 shows a typical simulation result for the residual current Is (blue) into the IC at a total ESD current It (red) for a 4 kV gun discharge. A residual current Is ≈ 12 mA remains after the external protection for this particular configuration. In the same way, the residual voltage at the IC pin can be simulated. By comparing residual current and voltage with the known failure levels for the IC, the system robustness can be simulated. An example for a real application will be given below.

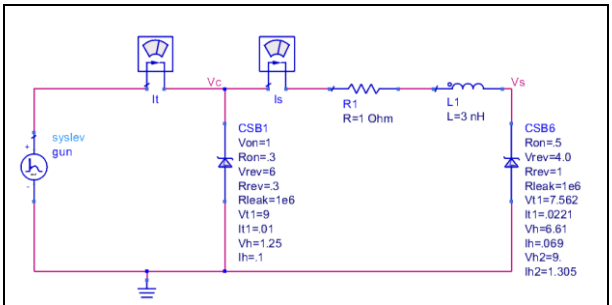

Figure 8 System-Level Simulation (SEED)

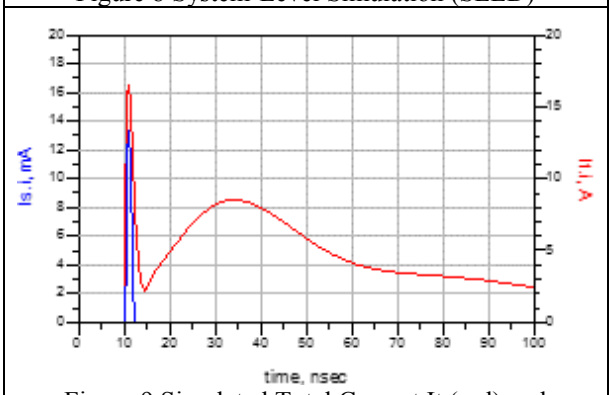

Figure 9 Simulated Total Current It (red) and Residual Current into the IC Is (blue).

CALIBRATING THE MODEL

Before the system robustness can be calculated, we need to calibrate the clamp parameters. The calibration is performed using Transmission Line Pulse (TLP) measurements (Maloney et al. 1985), which has the advantage that it provides a square current pulse with a flat 100 ns plateau (cf. Figure 7) as opposed to a gun pulse which has a double exponential waveform (cf. Figure 9). It has been shown (Notermans et al. 2012) that TLP measurements correlate well with gun discharge measurements, as far as thermal failure is concerned.

Clamps

Figure 10 shows a comparison between simulated and (TLP) measured I-V curves. The calibration is performed by entering the (V,I) points for the inflection points, as discussed in the previous section. It is easy to extend the model with additional inflection points, if required, e.g. to model thermal effects for high currents as well.
Figure 11 shows a zoom-in of the I-V curve of Figure 10 to highlight the fit for small currents. In the simulation a leakage resistor of 1 MΩ is used, which facilitates convergence. In reality, the leakage current maybe well below 1 nA, but for ESD simulation purposes the very low current behavior is not important.

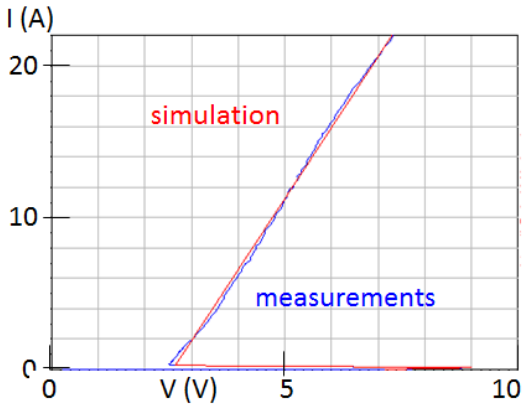

Figure 10 Comparison of Simulated and Measured (TLP) I-V Curve

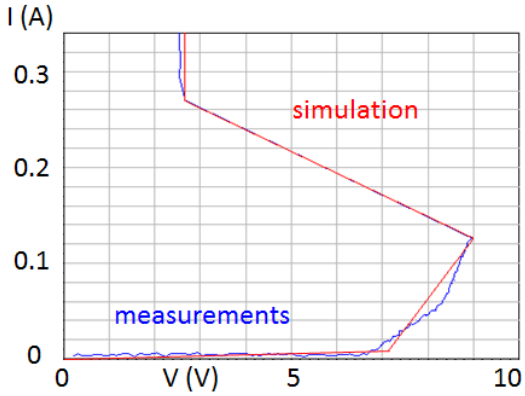

Figure 11 Zoom of I-V curve in Figure 10 for low Currents

Parasitics

For a complete system simulation, the parasitics of both (IC) internal and external protections, as well as the system board need to be determined.

Capacitance

The capacitance of the external protection is either measured directly using an Agilent E4980A precision LCR meter, at 1 MHz, or extracted from S-parameter measurements using a Rohde & Schwarz ZVA40 Vector Network Analyzer, up to 40 GHz.

For high-speed applications, such as USB3, typical capacitance is about 0.25 pF or less.

Inductance

Measuring the parasitic inductance is usually a bit more complicated. One possibility is to measure the S21 parameter and extract the capacitance at low frequency. From the resonance frequency and the known capacitance, the inductance can be derived. Typical inductances for external protections range from about 0.1 nH for CSP packages to about 1.5 nH for wire-bonded packages. Similar values are usually obtained for the IC, depending on the package type as well.

TLP Inductance measurement

In case RF extraction is not possible, e.g. due to too many reflections, the inductance may be estimated using TLP measurements and plotting the measured inductive over-voltage against dI/dt. If the relation is linear, the slope of the resulting line is the inductance L.

Figure 12 shows the peak voltage in a very fast vf-TLP pulse of 5 ns width in a protection device. The risetime of the current pulse is 0.6 ns. For high currents, the curve becomes linear and the slope corresponds to the inductance of the device, according to L = Vpeak/(dI/dt). For this example, an extracted L ≈ 0.75 nH results. The non-linear part below 10 A is caused by the conductivity modulation part, which is described elsewhere (Notermans et al. 2018).

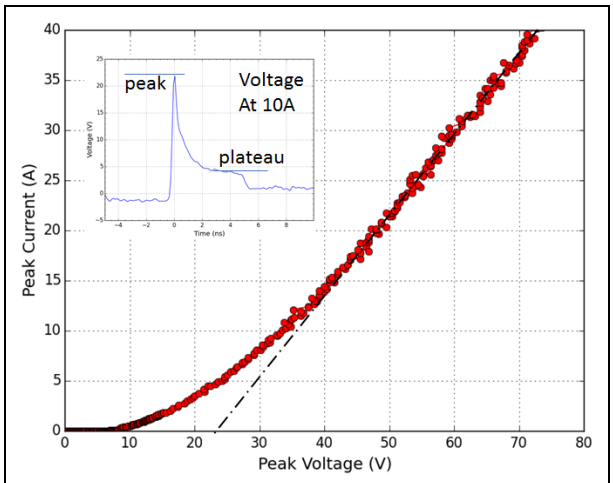

Figure 12 Peak (=Overshoot) Voltage versus Current

ESD CURRENT FLOW

It may not always be obvious which board components need to be included in a SEED simulation. It is, therefore, helpful to use a current spreading tool to determine the ESD current flow. We have used an Amber Precision SmartScan ESD-350 to show the ESD current on the USB3 board using a magnetic field probe. Figure 13 (left) shows a scan of the board with the original on-board protection set-up. The connector is at the bottom right. A first protection (prot1) is connected directly behind the connector, followed by a 1 Ω resistor and a second protection (prot2). The scan shows that the residual ESD current enters the IC at the RX1 pin. Part of the residual current is absorbed in the internal protection, but part of it exits the IC at a Vdd pin and flows via the decap to ground. The bottom graph shows that the maximum H-field is about 20 A/m.

The original protection scheme comprises two on-board protections and a 1 Ω resistor in a PI-configuration, presumably in an effort to improve the system protection. A second H-field scan, after the second protection was removed (Figure 13 right) reveals, however, that placing a second protection is actually counterproductive: more current is flowing into the IC (Figure 13 left).

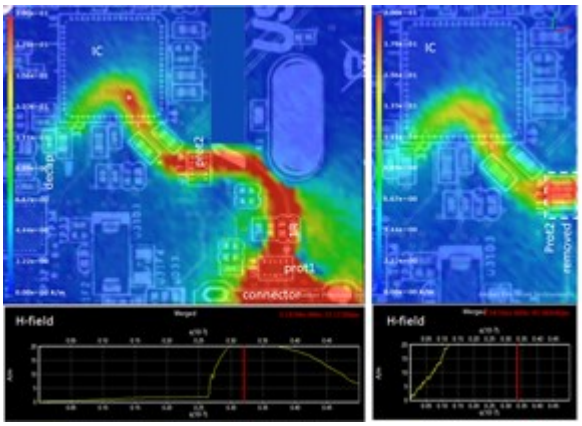

Figure 13 ESD Current on USB3 Interface with Double Protection (left) or Single Protection (right)

This example illustrates that the H-field scanner can be a valuable tool to assess the effectiveness of a proposed system protection scheme.
The residual ESD current is, in fact, strongly related to the inductance of the protection and, thus, to the overshoot (cf. Figure 12 inset) during an ESD (or TLP) pulse.

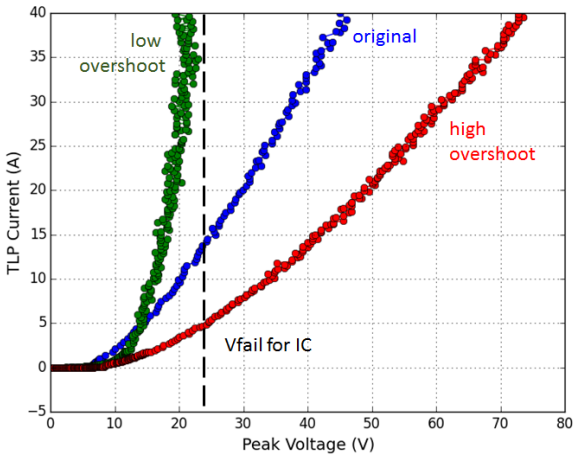

Figure 14 Peak Voltage against current for several Protections

Figure 14 shows the TLP peak voltage vs. TLP current for several on-board protections (alone). The original protection (blue) is compared with a protection with a lower overshoot voltage (green) and one with a higher overshoot voltage (red).
When the original on-board protection is replaced by a protection with a higher overshoot the residual current into the IC increases (Figure 15 left) compared to Figure 13 (right) and, conversely, using a protection with a lower overshoot reduces the residual current (right).
In fact, since the voltage for the low-overshoot device (PESD2V0Y1BSF) levels off around 22 V, which is lower than the failure voltage of the IC, the system ESD performance is in this case limited only by the ESD robustness of the protection (> 15 kV).

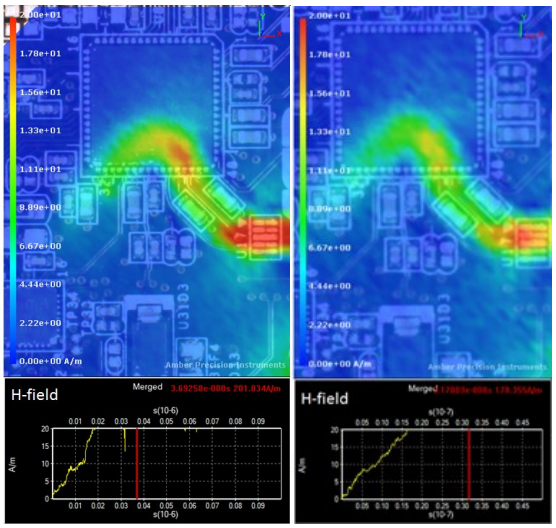

Figure 15 Protection with Higher (left) and Lower (right) Overshoot Voltage.

USING SEED ON A USB3 INTERFACE

The suitability of the SEED approach can be demonstrated on a USB3 PCIExpress board for a PC. Figure 16 shows the test set-up, which has been described in detail earlier (Notermans et al. 2016). The USB3 card is put into a PCIExpress slot of a PC and the gun is fired directly into one of the two receiver (RX) pins on the USB3 socket.

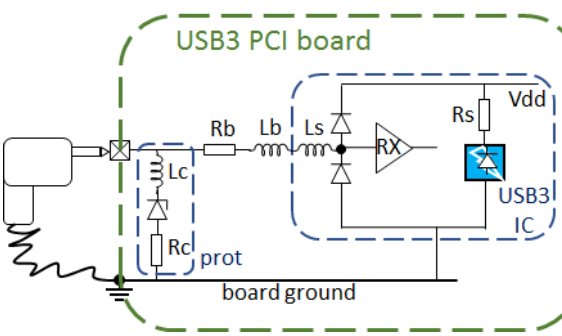

Figure 16 Gun Test on USB3 PCI Board.

The USB3 IC has a rail-based internal protection, with dynamic resistance Rs and parasitic inductance Ls. On the board there is an external protection with dynamic resistance Rc and inductance Lc, a resistor of Rb = 1 Ω and parasitic inductance Lb. The (parasitic) capacitances have not been included, because they are very small (typically < 0.25 pF) to allow a high bandwidth of > 10 GHz. Such small capacitances have negligible impact on the outcome of the SEED simulation. Of course, they would need to be included in a simulation under normal operating conditions.
It has been shown before (Notermans et al. 2016) that system performance is limited by the residual current into the IC during the fast first peak (cf. Figure 3) of the gun discharge. During the slower second peak the residual current is determined by the ratio of the dynamic resistances in the external vs. the internal protection:

Rc/(Rb+Rs).
During the first peak, however, the impedance of the inductances is much larger than the ohmic resistances and the residual current is determined by the ratio of the inductances Lc/(Lb+Ls).
This effect is illustrated in a measurement of a 1 kV gun discharge for three different inductance ratios (Figure 17).

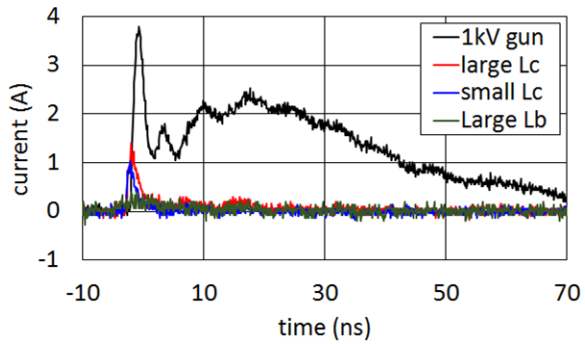

Figure 17 Residual Current Waveforms for three Inductance Ratios, compared to the Gun Waveforms

The current waveform of the gun is shown in black and the residual current for a relatively large Lc = 1.3 nH (red), Lc =0.7 nH (blue), and a very large LB = 35 nH (green) is compared. It is clear that the second peak is well suppressed in all cases, but a significant residual current remains during the first peak, which is highest for a large Lc (37%), followed by a small Lc (27%). The best solution is obtained when a large inductance Lb is added in the path to the IC (< 10%). The ESD performance scales accordingly (Notermans et al. 2016).
The effect of the inductive current distribution can be simulated using a SEED model (Figure 18). The correlation with measurements is excellent. The simulated residual current scales with the Lc/(Lb+Ls) ratio, as in the measurements.

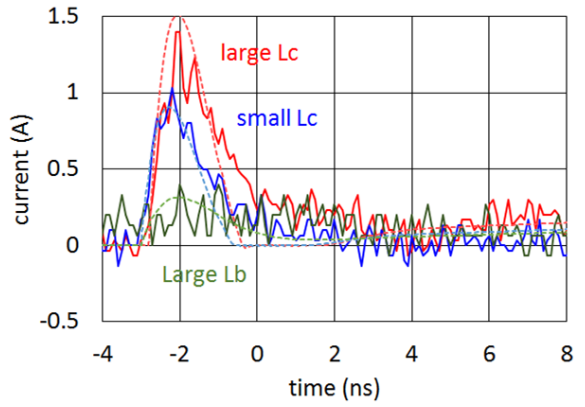

Figure 18 Measured (solid) and Simulated (dotted) Residual Current in the First Peak for several Lc/(Lb+Ls) Ratios

Note that the large inductance Lb = 35 nH is introduced into each of the two differential RX lines. The two air coils are coupled in such a way that the effective differential inductance is close to zero. Thus, the differential USB3 signal passes undamped. But an ESD signal couples to both lines as common mode signal and experiences the full inductance in each line (Werner et al. 2015 and 2016).
The measured and simulated peak currents in the first peak are summarized in Table 1. The correlation is very good.

Table 1 Comparison of Simulated and Measured First-Peak Current Amplitudes of Figure 17

1st peak (A)	measured	simulated
gun	3.76	3.64
large Lc	1.40	1.42
small Lc	1.03	0.86
large Lb	0.33	0.32

CONCLUSION

The paper has presented quasi-static Verilog-A models for the on-chip and on-board protections in a system. An H-field scanning tool may provide essential insight in where the residual current is flowing during a system level discharge, which facilitates setting up a complete system model.
The complete circuit model, incorporating these models allows accurate prediction of the system-level ESD performance.

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