CALCULATING THE VOLTAGE ACROSS A TURNED OFF SEMI-CONDUCTOR MODELLED BY PERFECT SWITCHES

Faouzi BOULOS
Department of Physics
University Lebanese of Science II
Fanar BP 90656, Jedeidet-El-Maten, Lebanon
Email: faboulos@ul.edu.lb

KEYWORDS

Semi-conductor modeling, power electronic circuits, numerical simulation, variable topology method.

ABSTRACT

The aim of this paper is to describe a numerical simulation method of power electronic circuits. The problem of the method is due to the fact that the semi-conductors are simulated by perfect switches. That is two nodes connected by a conducting semi-conductor are merged, and two nodes connected by a turned off semi-conductor have their branch removed, sometimes leaving some nodes pending. The branches terminated by pending nodes are also removed. A method, which will be shown further is based on a topological analysis of the circuit allowing the extraction of the relations and the calculation of the voltage across a turned off semi-conductor. The method consists of simplifying the initial figure of the circuit and setting up the mathematical formulation and development of the automatic simulation.

INTRODUCTION

The choice of the electric model of the semi-conductor is thus very important. There are several ways to represent the semi-conductor which are all electrically equivalent (Antognetti and Massobrio 1988). Similarly, all semi-conductors may be represented by equivalent electric circuits more or less complex, which can be used in the electronic circuit simulation for example (Nagel and Pederson 1973). Some of the most frequently used models are:

binary variable resistance, depending whether the semi-conductor is "off " (high resistance) or "on" (low resistance). Controlled voltage source or current source (Laktos 1979), inductance in series with a parallel RC circuit (Rajagopalan 1978), inductance and resistance (Eisenar and Hofmenister 1972).

In these cases the topology is fixed, the circuit and the size of the calculating matrix is fixed. Another method is to represent the semi-conductor by replacing it by an open circuit when it is "off" and by a short circuit when it is "on". Thus, the topology is variable. Each condition has its set of equations, which reduces the size of the calculating matrix considerably (Boulos 1988). On the other hand in the variable topology method the semi-conductors are simulated by perfect switches, the circuit

and the equation system are variable (Boulos 1988). The difficulty is due to the fact that in such a method the semi-conductors are simulated by perfect switches, that is two nodes connected by a conducting semi-conductor are merged and two nodes connected by a turned off semi-conductor have their branches removed, sometimes leaving some nodes pending. The branches terminated by pending nodes are also removed. This point is resolved by an algorithm (Boulos 2001); that makes it possible to modify the complete topology of the circuit at each sequence of operation. This makes the knowledge of the current in a conducting semi-conductor and the knowledge of the voltage across a turned off semi-conductor difficult to obtain. In a previous publication (Boulos 2002), I have presented a solution for the method based on a topological analysis of the circuit allowing the extraction of the relations calculating the current in a conducting semi-conductor. In this paper I present solutions for the extraction of the relations and the calculation of the voltage across a turned off semi-conductor.
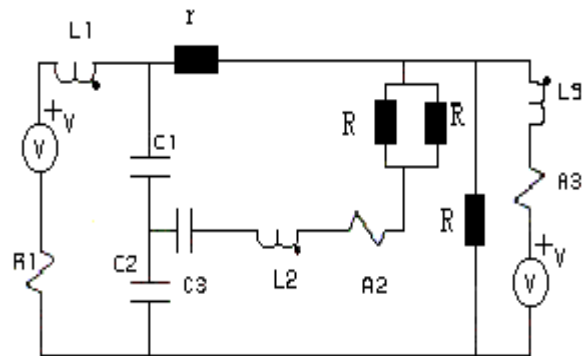
THE FIXED TOPOLOGY METHOD

Figure1: The semi-conductor is "off " (high resistance R) or "on" (low resistance r).

In this type of simulation, the circuit is fixed and the equation system is unique, yet, some values of the coefficients may change according to the operating point of the semi-conductors. They are considered high resistance when they are "off" (R) and low resistance when they are "on" (r). For the principal function, see figure 1.

THE VARIABLE TOPOLOGY METHOD

In the variable topology method, the semi-conductors are simulated by perfect switches, shown in figure 2. When the semi-conductor is "on", we link the two nodes by a semi-conductor, when the semi-conductor is "off"; we take off the link between the two nodes.
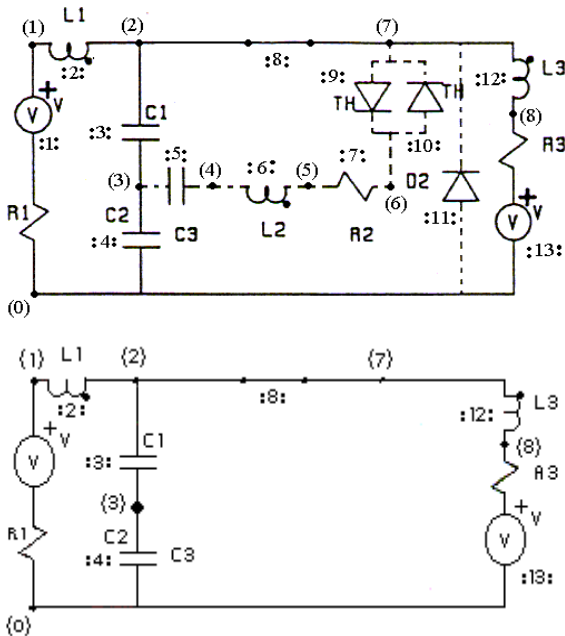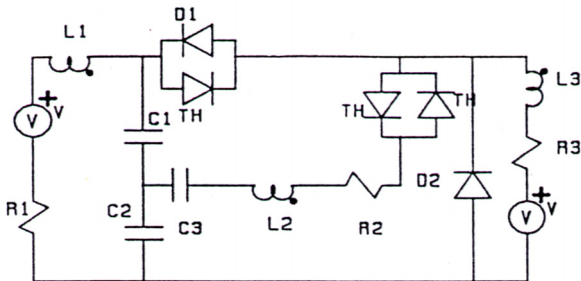

Figure 2: The semi-conductors are simulated by perfect switches.

At each step, the topology of the electric circuit is simplified compared to the original circuit. The number of differential equations is lower than the one obtained by the fixed topology simulation. Main difficulty of the general variable topology method: this method makes the knowledge of the voltage across a turned off semi-conductor difficult to obtain. The algorithm resolves this point it is possible to modify the complete topology of the circuit to each sequence of operation.
That is to say the figure 3 with:
(E) Is the whole of information represented tables and which relates to the configuration of the circuit (standard elements, numbers of the branches and nodes, state of the semiconductors, value of the voltage of all the capacitive branches and generators of voltage and value of the current of the inductive branches and generators of current). After passage of this information in "

TOPOVAR ", we obtain at the exit the information used during all this phase of operation as follows:
- (S1) which represents the form of minimal topology with a new classification and which allows us the setting in automatic equation.
- (S2) which is a whole of vectors and tables enabling us automatically to know the blocked value of the terminal voltages of the semiconductors.
- (S3) which is a whole of vectors and tables allowing us to know the value of the currents automatically which crosses the conducting semiconductors.
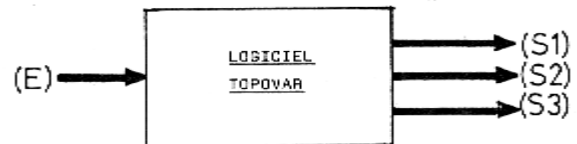

Figure 3: The "TOPOVAR".

The main steps of this algorithm
1. Remove automatically all turned off semi-conductors and all branches leading to pending nodes.
2. Short circuit conducting semi-conductors.
3. Determine automatically at each step the new number of all the nodes that are either anode or cathode of turned off semi-conductors in order to know the voltages across those semi-conductors.
4. Determine automatically at each step the number of the branches connecting the anode nodes, and the number of the branches connecting the cathode nodes of a conducting semi-conductor, in order to know the current in the semi-conductor.
5. Determine automatically the form of the minimal topology. This topology contains a new number of nodes and branches. After applying the algorithm, only passive elements such as resistances, self-inductances, capacitors, voltage and current generators remain present in the structure figure 2.

GENERAL PRESENTATION OF THE METHOD SUGGESTED

From the data (topology and components) and for each phase of operation, it is necessary to determine minimal topology, the new value of the nodes of entry and exit of the semiconductors after removal of the branches traversed by a null current and the value of the voltage for each blocked semiconductor.

AUTOMATIC REMOVAL OF THE BLOCKED SEMICONDUCTORS AND OF THE BRANCHES ENDING BY PENDING NODES

Consider a complete circuit containing a certain number of active and passive branches. For each blocked semi-conductor, one removes the corresponding branch.
Then the nodes of input and output are separated, which gives a circuit with two parts: a side node for the input, and another for the output figure 4. The main problems to be solved at this stage are:

1) Determination of the new numbers of nodes of input and output for each blocked semiconductor (and removed) when there is removal of branches in series, terminated by pending nodes.

2) Determination of the value of the terminal voltage of each semiconductor removed. This value can depend on the voltage of the removed branch if it is capacitive or if it contains a voltage source.
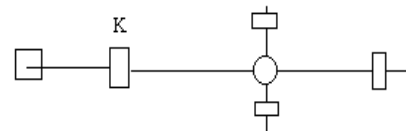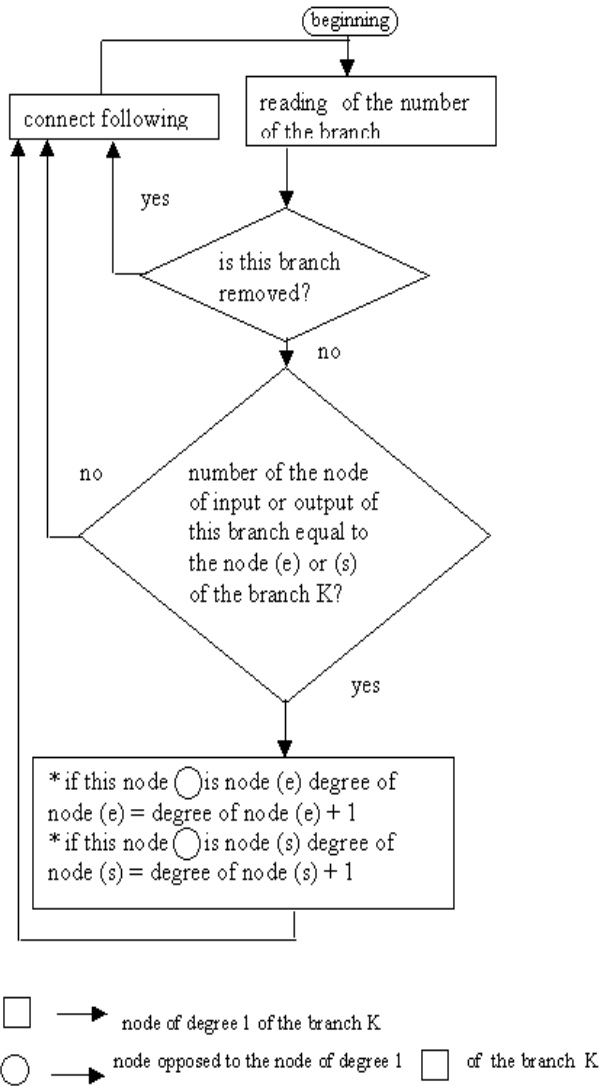

Figure 4 : The flow chart above presents the search for degree of the node opposed to the branch K connected to a node of degree 1.

AUTOMATIC DETERMINATION OF THE NEW NODES OF INPUT AND OUTPUT FOR EACH REMOVED BLOCKED SEMICONDUCTOR

This is done in a first step analysing the circuit branch by branch and remove every branch containing a blocked semiconductor. In a second step the process is repeated checking we seek if the output of this branch is equal to the input node (e) of the blocked semiconductor.

a) If so, we keep the number of this branch and assign a degree for the node (e) = degree of the node (e)+1.

b) If not, we seek if the input of this branch is equal to the node (e)

-If yes we keep the number of this branch and we assign a degree for the node (e) = degree of the node (e) +1.

- If not, we move to the next branch.

The same process is repeated for the output node (s).If the degree of the node (e) or the node (s) is equal to 1, the branch that connects this node is pending and this branch is removed. When the degree of the node is not equal to 1, this node is the new number for this blocked semi-conductor which is stored in the matrix G (X, Z).

AUTOMATIC DETERMINATION OF THE VOLTAGES ACROSS BLOKED SEMI-CONDUCTORS

The objective is to determine the voltage across each blocked semiconductor. It should be noted that the search for the new input and output nodes is not sometimes sufficient to know the variation of the voltage across the removed blocked semiconductors for each branch containing a capacitor or a voltage source contributes to the determination of this voltage. For that, we will show how, starting from the removed passive branch we calculate the value of the voltage across each blocked semiconductor. We start by defining a function f (X, Y) which determine the terminal voltage of each blocked semiconductor.

$$f (X, Y) = VC (X, Y) + VE (X, Y) \qquad (1)$$

With:

X = number of branch containing a blocked semiconductor,

Y = 1 or 2 according to whether one works on the corresponding node output or the node input of the blocked semiconductor at each instant of time, we are able to define the values of the functions f (X, 1) and f (X, 2). These two functions allow is to know the voltage across each blocked semiconductor by applying the following relation:

$$F(K)=(U(G(K,2))+f(K,2))- (U(G(K,1))+ f(K,1)) \qquad (2)$$

With:

F (K): Voltage across the blocked semiconductor numbered K.

U (G (K, 2) + f (K, 2) Voltage of the input node (E) of the blocked semiconductor compared to the reference node (O)

U (G (K, 1)) + f (K, 1) Voltage of the output node (S) of the blocked semiconductor compared to the reference node (O). It should be noted that at each step of

calculation the value of the voltage of each blocked semiconductor must be calculated.

We study now the construction of matrices VC (X, Y) and VE (X, Y).

Case of the capacitive branches VC (X,Y).

Each capacitive branch connected to a node of degree 1 is removed. The value of the voltage accross these terminals is stored in VC (X, 1) for output node of the blocked semiconductor numbered X and in VC (X, 2) for the input node of this blocked semiconductor.
For example:

-   VC (X, 1) = VC (X, 1) + F (K)   (3)

-   VC (X, 2) - VC (X, 2) + F (K)   (4)

During a whole phase of operation, the values of VC (X, 1) and VC (X, 2) remain constant. However, for each new phase of operation the matrix is initialized with zero value. We analyse in order to better understand the step to study the example of the chopper drawn figure 2 We are interested in the phase of operation during which thyristors of branches :9: and :10: as well as the diode of branch :11: are blocked whereas the switch of branch :8: is conducting and the capacitor of branch :5: is pending. The voltage across its terminals acts on the input node of branch :10: and the output node of the branch :9: . We will seek for the blocked semiconductor numbered 9 of which its side of the node of entry or node of exit depends the tension of the capacitive branch number :5: is pending. We find that it is the node of exit of the branch :9: that takes the value of the node of entry of the capacitive branch numbered :5:, then VC(9,1) = VC(9,1) +F(5).
For the blocked semiconductor of the branch :10:, it is the node of entry which becomes equal to the node of entry of the capacitive branch numbered :5:.
Therefore: VC (10,2) = VC (10,2) +F (5)

Case of the voltage source

The difference between a capacitive branch and a branch containing a voltage source comes owing to the fact that the tension of a voltage source can vary as a function of time. Thus, its value is F(K) = VM(K) where VM(K) is the amplitude of the voltage source. It is thus necessary to recompute the voltage source for each step of calculation and to store it in VE(X,Y).

AUTOMATIC DETERMINATION OF THE VALUE OF THE CURRENTS THAT CROSS EACH REMOVED CONDUCTING SEMI-CON-DUCTOR

The current in a semiconductor is the algebraic sum of the currents of the branches that connect the input node or the output node. It is to be noticed that the knowledge of the information stored in matrices MAENT (X, X1), MASORT (X, X1), SIGC (X, X1) enable us automatically to know the value of the currents which at every moment cross all the conducting semiconductors of calculation. For that, we apply one of two following equations:

$$ISC(X)= ISC(X)+SIGC(X,X1)*IBB(MASORT(X,X1)) (5)$$

$$ISC(X)= ISC(X)+ SIGC(X,X1)*IBB(MAENT(X,X1))   (6)$$

With:
ISC(K) Vector containing the value of the current of the conducting semiconductor number K.
SIGC(X1,X2) Matrix containing the values of the signs of the current that cross the branches connected to the input node or the output node of a conducting semiconductor. (n) Number of node and :n: number of branch.
MAENT(X1,X2) Matrix containing the numbers of the branches related to a conducting semiconductor on the side of the input node with: integer variable X2 varying from 0 with the maximum number of branches connected to this node.
MASORT(X1,X2) Even definition that MAENT(Xl,X2) but for the output side.

FORMING AND SOLVING THE EQUATIONS

In order for the program to be automatic, it must establish the equations by itself. This is achieved in two steps:
the first step consists of the topological study of the circuit, and the second step consists of establishing the equations. An electronic circuit is represented by a group of branches connected together and the equations are established using mathematical techniques. This enables the analysis of a great number of different circuits, for which the formation and solving of the equations would otherwise require long and tiring calculations. It is not possible to list all mathematical techniques and numerical calculations in this article. Only the most frequently used methods will be mentioned, without going into detail   (Chue L.O. and Lin P.M. 1975) and (Pelletier 1971): nodal method, state variable method.
For the application, we chose the setting in equation by the nodal method for it asks less memory.

Nodal analysis method

Several simulators use this method, which is based on the solution of the matrix associated to the equations representing the electronic circuit. The matrix is solved by the method of the pivot. SPICE (Antognetti and Massobrio 1988). The nodal analysis method is used by several simulators because it is simple and powerful.
In this method, the equation system is in the form of:

$$(I) = (G)*(V)   (7)$$

(I) Vector of electrical current.

(V) Vector of the voltages of the nodes compared to the reference nodes.
(G) Matrix of the admittance.

THE PRINCIPAL OF THE SIMULATION SOFTWARE AVARIABLE TOPOLOGY METHOD
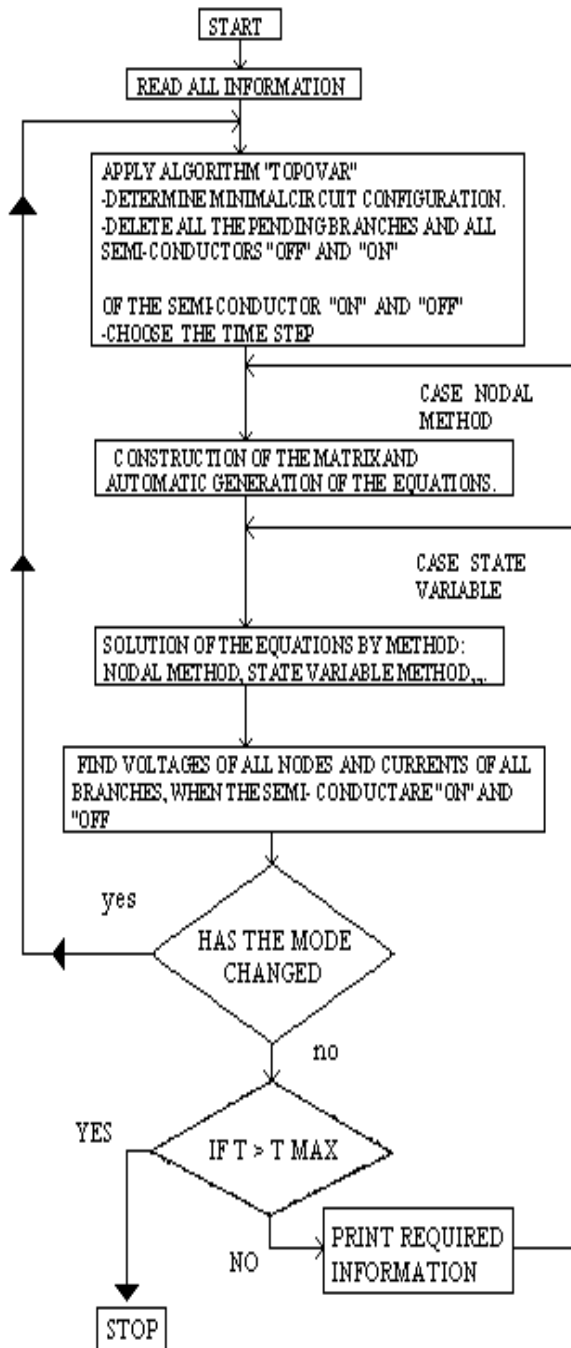

Figure 5: General flow-chart for variable topology.

RESULTS

In order to illustrate the mentioned methods, the results obtained by simulating a chopper figure 6 are shown.
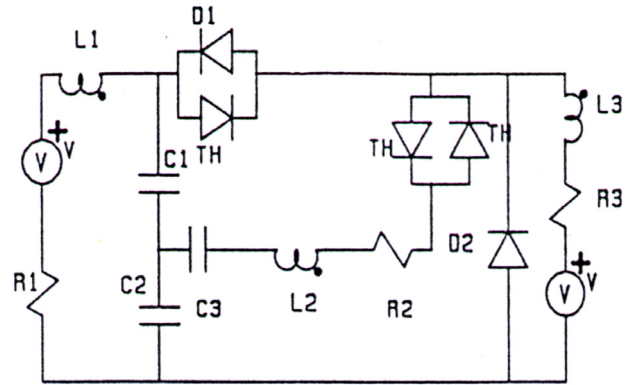

Figure 6: Schema of the simulated chopper.

The states of the semiconductors are represented by 0 for the semiconductors that are "off" and 1 for the semiconductors which are "on"..

$\overline{W}$ (n-1,n): Represents the calculation matrix corresponding to the minimal topology having (n-1) lines and (n) columns.

δt: Is the simulation time used for $\overline{W}$ (n-1,n) during a simulation period 2.10^{-4} s

For: D2 TH1 TH2 THP
T=0.000E+0   1   0   0   0 => VD=8 , $\overline{W}$ (4,5)
T=1.000E-5   1   0   0   1 => VD=9, $\overline{W}$ (4,5)
T=1.376E-5   0   0   0   1 => VD=1, $\overline{W}$ (6,7)
T=3.000E-5   0   0   1   1 => VD=3 , $\overline{W}$ (4,5)
T=5.927E-5   0   0   0   1 => VD=1 , $\overline{W}$ (6,7)
T=1.200E-4   0   1   0   1 => VD=5 , $\overline{W}$ (7,8)
T=1.513E-4   0   1   0   0 => VD=4 , $\overline{W}$ (6,7)
T=1.733E-4   1   1   0   0 => VD=12 ,$\overline{W}$ (4,5)

We regard a thyristor and an antiparallel diode as only one switch THP.
Table I shows the time ratios obtained when using the example of the chopper figure 6. The gain is between 2 and 3.

Table 1: The time ratios obtained.

$\dfrac{\overline{W}()}{\overline{W}()}$	$\delta_{n}\%$	$\delta_{t}\mu_{s}$	$\mu_{=\overline{TT}}\dfrac{\delta t}{}\%$
$\dfrac{(20)}{(72)}$	27%	$95\mu_{s}$	47,5 %
$\dfrac{(42)}{(72)}$	58%	$75\mu_{s}$	37.5%
$\dfrac{(52)}{(72)}$	77%	$30\mu_{s}$	15 %

Where:
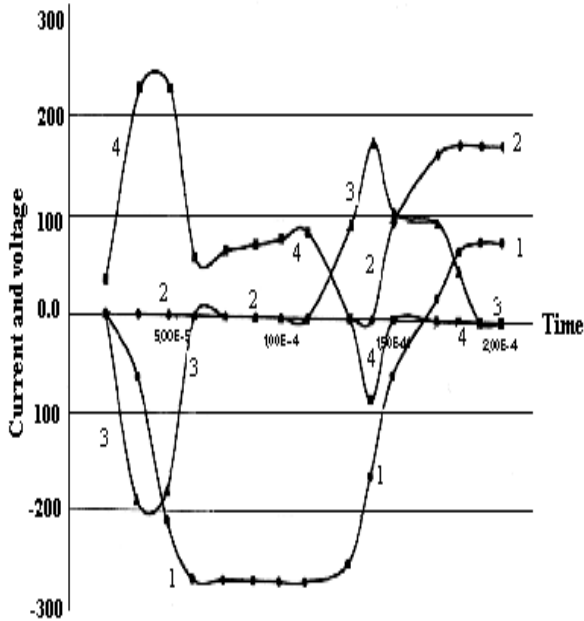$\overline{W}$ (n-1,n): calculating matrix corresponding to the minimal topology.

W(n-1,n): calculating matrix corresponding to the fixed topology.

$\delta_n\%$: Percentage of the number of elements used for the variable topology.

δ_t: Simulation time for $\overline{W}$ (n-1,n) during a certain simulation period.

μ: Percentage of the simulation time.

TT: Simulation period.

1- Voltage across a condensator C3.
2- Voltage across a diod D1 and the antiparallel TH.
3- Current in a condensator C3.
4- Current in a diod D1 and the antiparallel TH.

Figure 7: Represents the results of the simulation using the variable topology.

We present the form of the currents and the tensions for the capacitive branch C3 and the diode D1 and the antiparallel thyristor TH.

CONCLUSION.

The aim of this article was the study and the realization of a general program of numerical simulation of static inverters by the method of variable topology. The characteristic of this method is the representation of the semiconductors in the form of perfect switches. Work was carried out in two stages. The first stage is the determination of minimal topology according to the state of the semiconductors. Then the reconstitution of the terminal voltages of the blocked semiconductors is removed. The second stage is the setting in automatic equation and the resolution of these equations.

The advantage, which this modeling type brings, is a notable simplification of the system of equation to be solved. The secondary time constants of the modeling

semiconductor by fixed topology are avoided, which implies that an execution time of variable topology is simulation is shorter and result of simulation more precise.

REFERENCES

Antognetti P., G. Massobrio 1988. "Semi-conductor Device Modeling with SPICE" *McGraw-Hill Book.*

Boulos F. 1988. "Etude et réalisation d'un programme de simulation de convertisseurs statiques. Utilisation d'une méthode à topologie variable". *Thèse de docteur de l'Université Paris VI.*

Boulos F. 2001. " Numerical simulation of power electronic Circuit. Use of variable topology method. Modelling of the Semiconductor as parfect switches". *SCS MESM 3rd Middle East Symposium on Simulation and Modelling,* (September 3-5), PP. 97-100.

Boulos F. 2002. " Calculating the current in conducting semi-conductors modelled by perfect switches". *SCS MESM, 4th Middle East Symposium on Simulation and Modelling,* (September 28-30), PP. 217-222.

Chue L.O., Lin P.M. 1975 "Computer aided analysis of Electronic circuits" *Prentic-Hall New-Jerssay,*USA.

Eisenar H. and Hofmenister H 1972. "Digitale nachbildung von electrischen netz werken mit dioden und thyristoren "*archin fur Electrotechnik* n55.

Lakatos L. 1979. " A New method for simulating power semi-conductor circuits". *IEEE Trans. Ind. Electro.* Vont Inst. Vol IECI - 26 n 1 (Feb).

Nagel L. N., Pederson D-O.1973. *"SPICE"* Simulation program with integrated circuit emphasis*" Berkeley California: University of California Electronics Research laboratory* Memorandum ERL,M 382 (Apr 12).

Pelletier P. 1971. "Techniques numériques appliquées au calcul scientifique". *Masson.*

Rajagopalan 1978. "Simulateur digital des convertisseurs de puissance à thyristors" *Can. Elec. Eng. J.* n 1PP 5-10(Jan).

BIOGRAPHY OF AUTHOR

FAOUZI BOULOS was born in Byblos in Lebanon. He studied in France at the university of Pierre and Marie Curie (Paris VI). He obtained a thesis in electronics in 1988. He worked a few years in France and returned to Lebanon. Since 1995, he is professor at the department of physics of Lebanese University of sciences II. His e-mail address is: faboulos@ul.edu.lb